

Conventional Vertical Power MOSFET Device Structure

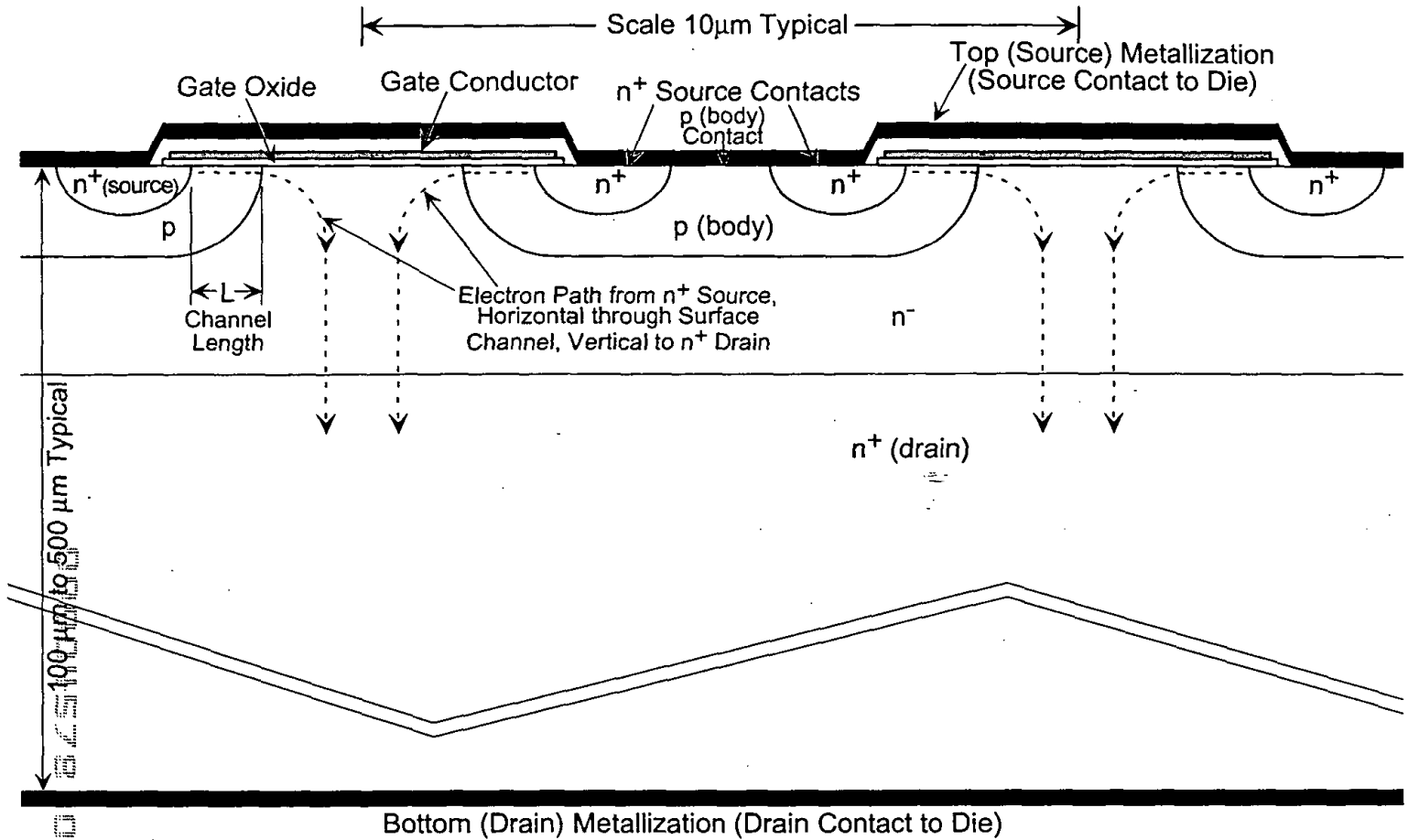


FIG. 1A

CMOS-Implemented Planar Geometry High Current Switching MOSFET Device Structure

Scale 2.0 μ m Typical

Note: Only M1(1st metal layer) shown; collection of all of the Source, Drain and Gate electrodes into High-Current Source and Drain Chip Contacts on M5 is accomplished in metal layers M2-M5.

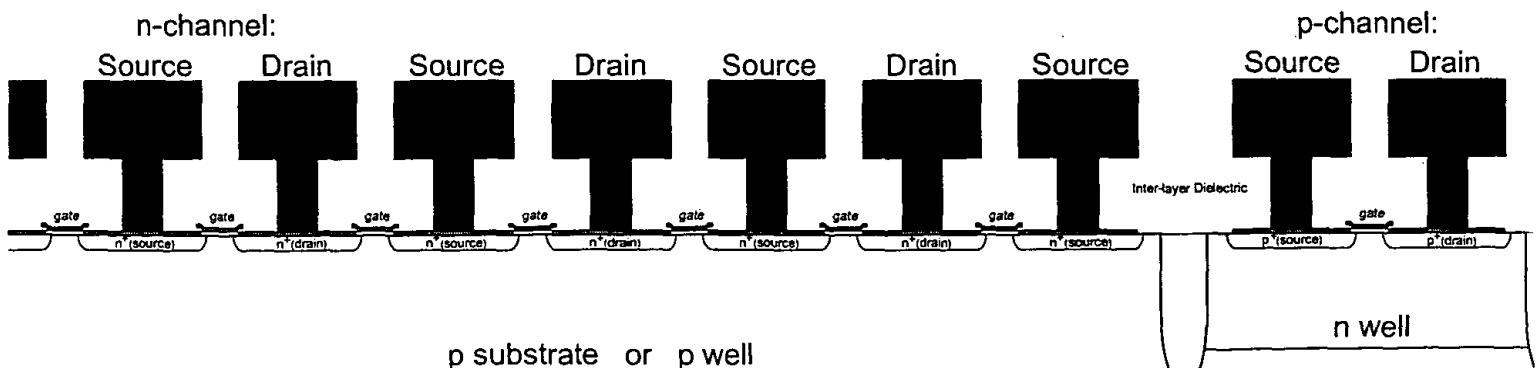
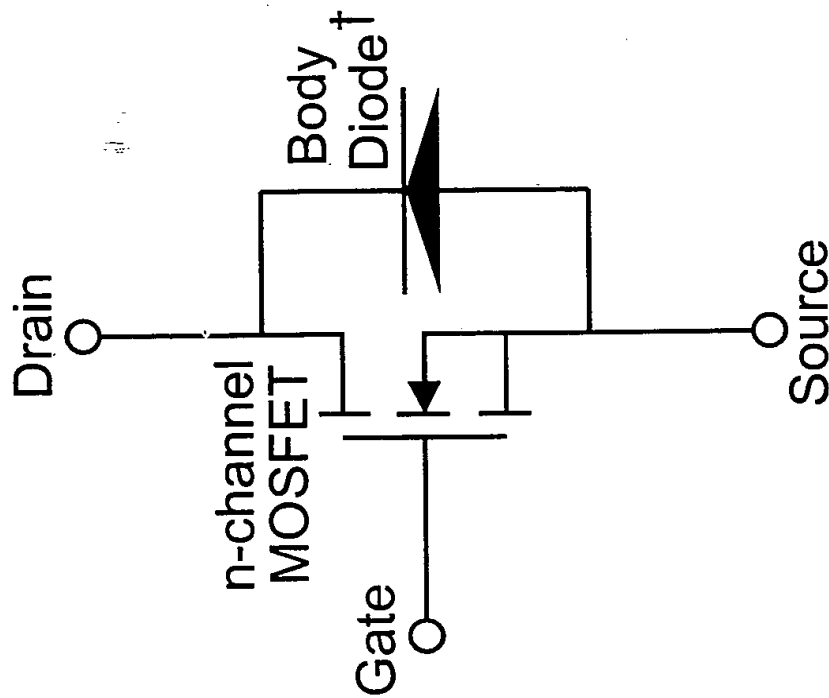


FIG. 1B

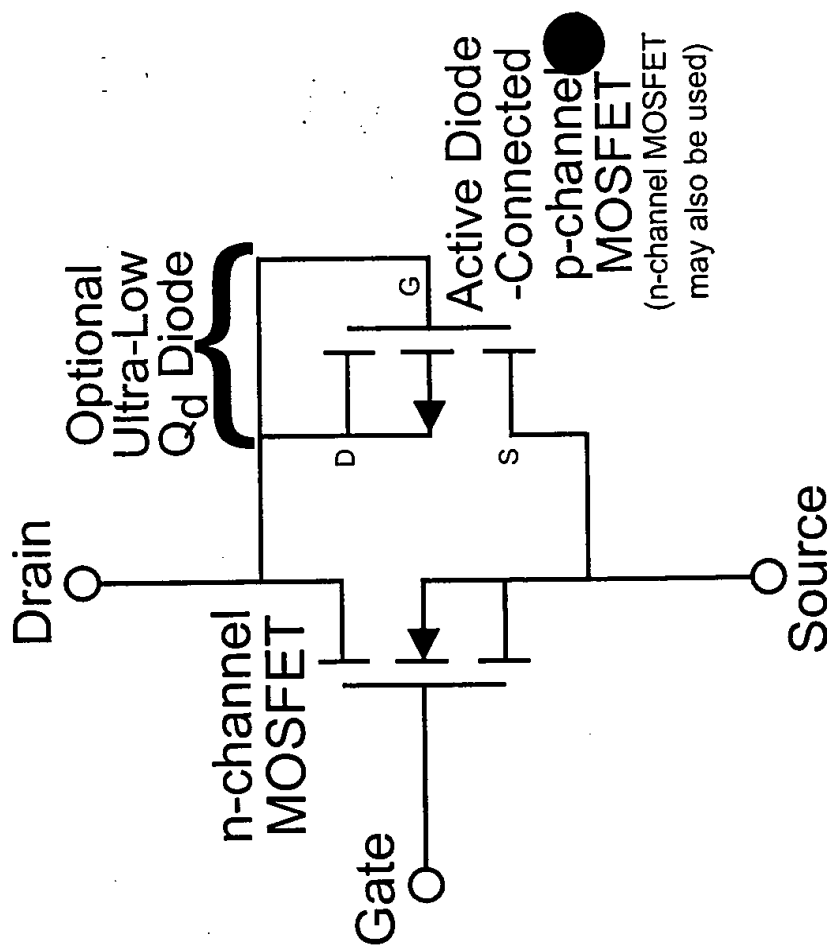
Conventional Power MOSFET Equivalent Circuit



[†] Note that Body Diode is a very large area p-n⁺-n⁺ diode with a very large diffusion charge storage capacity, Q_d . This means that when the body diode is first reverse biased after heavy forward conduction, a large transient reverse current, I_r , can flow for a substantial period of time, $t_r = Q_d/I_r$, which can limit usable switching frequencies.

FIG. 2A

CMOS-Implemented High Current MOSFET Equivalent Circuit



While a p-channel MOSFET with gate connected to Drain is illustrated, an n-channel MOSFET with its gate connected to the Source electrode will also serve as the active "body diode", turning on when the Drain electrode becomes more negative than the Source electrode by an amount greater than the threshold voltage, V_t , of the MOSFET. Note that if the Gate of the switching MOSFET is constrained to go no more negative than the Source, then it will, by itself, act as the "body diode".

FIG. 2B

Package

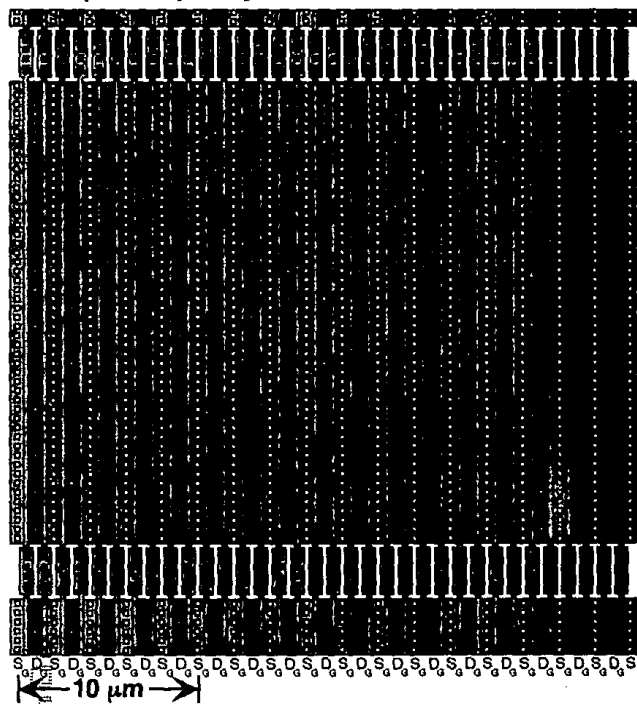


Silicon NMOS FET Substrate
(thickness not drawn to scale)

200 amp NMOS Switching FET Chip; Mask Levels M1-M3 & Poly

FIG. 4A

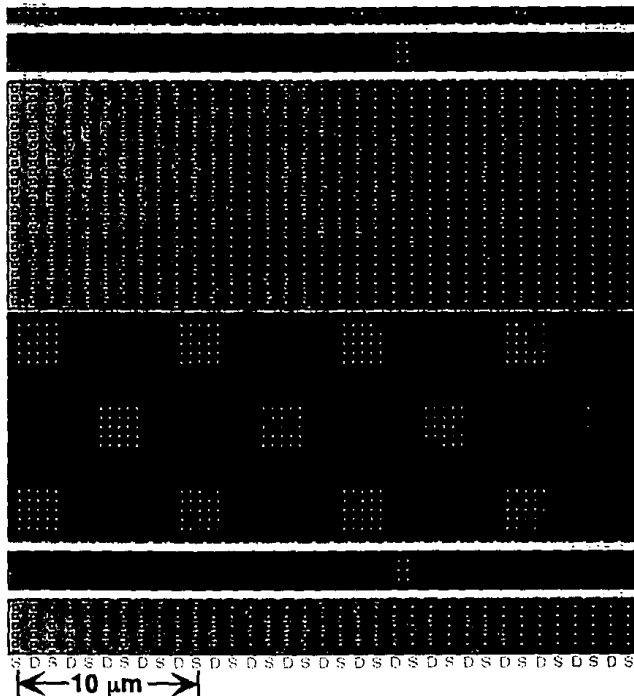
Source (Red)/Drain (Blue) Polysilicide and Gate (Green) Polysilicide with Vias to Metal 1



One complete 25μm high row of NMOS FET channel, with portion of rows above and below, is shown. Each row completes $W=250\mu\text{m}$ of NFET width in 10μm horizontal distance. S/D ohmic contact polysilicide (40Ω/Sq) shown in red for sources, blue for drains, with vias to Metal 1 (7.5Ω/cut) used to reduce current path resistance. Gate polysilicide (72Ω/Sq) is shown in green, with vias to M1 between rows.

FIG. 4C

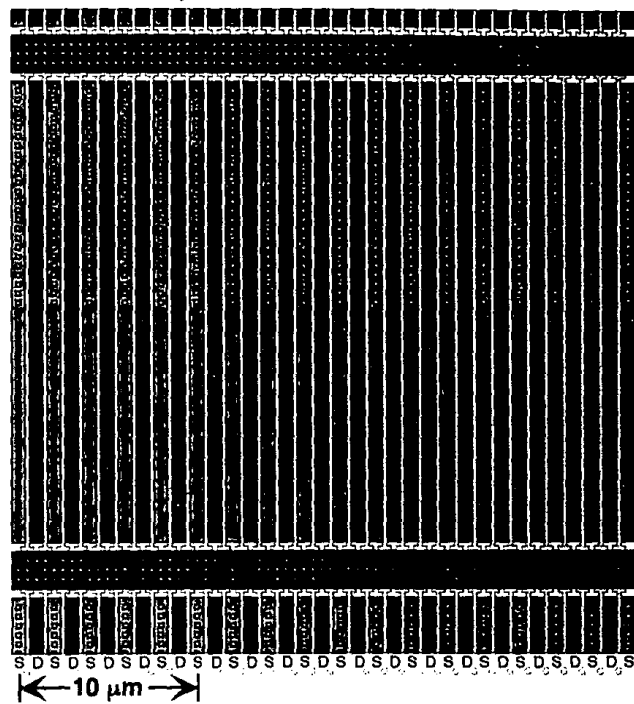
Source (Red), Drain (Blue) and Gate (Green) Metal 2 Busses with Vias to Metal 3 Plane



Horizontal source (red) and drain (blue) M2 (0.08Ω/Sq) busses tie the M1 source and drain stripes together. Since the next, M3, layer is a source plane, the source buss is completely covered with M2/M3 vias (5Ω/cut). The connections from the M2 drain busses to the M4 drain plane are done through an array of isolated M3 patches in the M3 source plane, so the drain buss M2/M3 vias are in patches as shown.

FIG. 4B

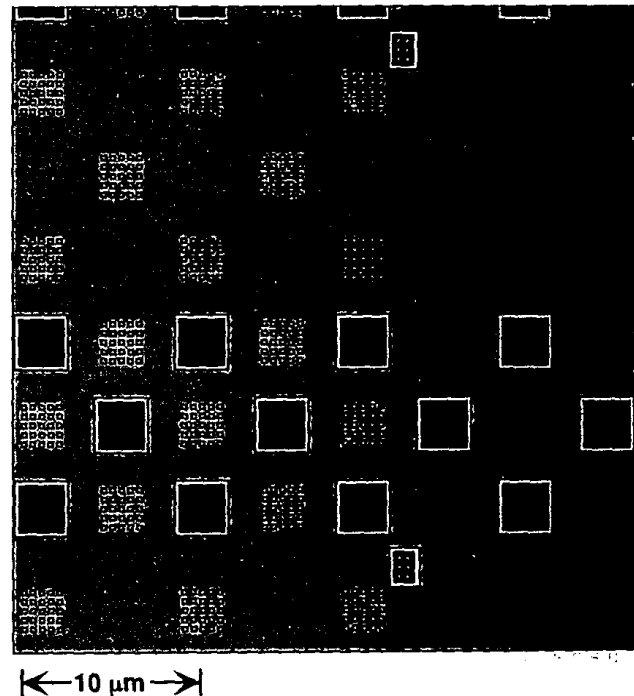
Source (Red), Drain (Blue) and Gate (Green) Metal 1 Jumpers with Vias to Metal 2 Busses



Metal 1 (M1; 0.08Ω/Sq) source and drain straps, $0.75\mu\text{m} \times 25\mu\text{m}$, are used to reduce resistance of S/D polysilicide in passing current to M2 horizontal S and D busses. Since source M2 buss is taken to cover the upper half of the 25μm channel, the source stripes (red) carry the current from the lower half of the channel to the M1 to M2 vias (5Ω/cut) on the upper half of the channel, and visa-versa for the drain stripes (blue).

FIG. 4D

Source Metal 3 Plane (Red) & (Blue) Drain M3 Feedthru Patches with Vias to Metal 4 Plane

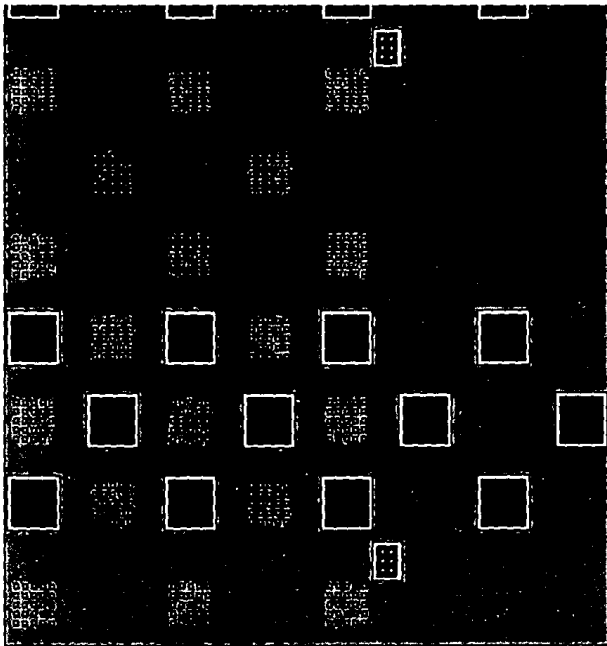


Metal 3 (0.08Ω/Sq) source plane (red) with isolated drain feedthru pads (blue) with M3/M4 via patches carrying current from the M2 drain busses to M4 drain plane. Left 22μm in area shown is under source M5 'checkerboard' pad contact area, so source plane has array of M3/M4 via patches going to isolated feedthru's in M4 drain plane. Right 13μm of area shown has drain M5, so here M3 carries source current laterally

200 amp NMOS Switching FET Chip: Mask Levels M3-M5 & Ball

FIG. 5A

Source Metal 3 Plan (Red) & (Blue) Drain M3 Feedthru Patches with Vias to Metal 4 Plane

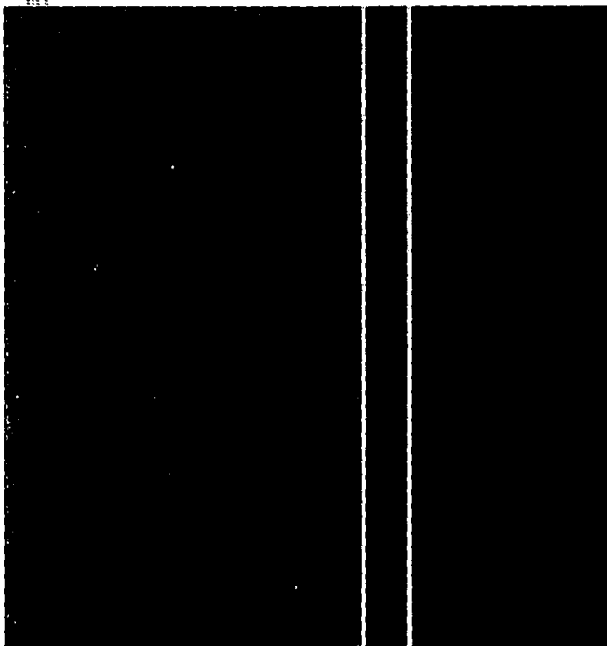


← 10 μm →

Metal 3 (0.08Ω/Sq) source plane (red) with isolated drain feedthru pads (blue) with M3/M4 via patches carrying current from the M2 drain busses to M4 drain plane. Left 22μm in area shown is under source M5 'checkerboard' pad contact area, so source plane has array of M3/M4 via patches going to isolated feedthru's in M4 drain plane. Right 13μm of area shown has drain M5, so here M3 carries source current laterally.

FIG. 5C

Detail of Part of 'Checkerboard' Source (Red) and Drain (Blue) Metal 5 Ball Contact Areas

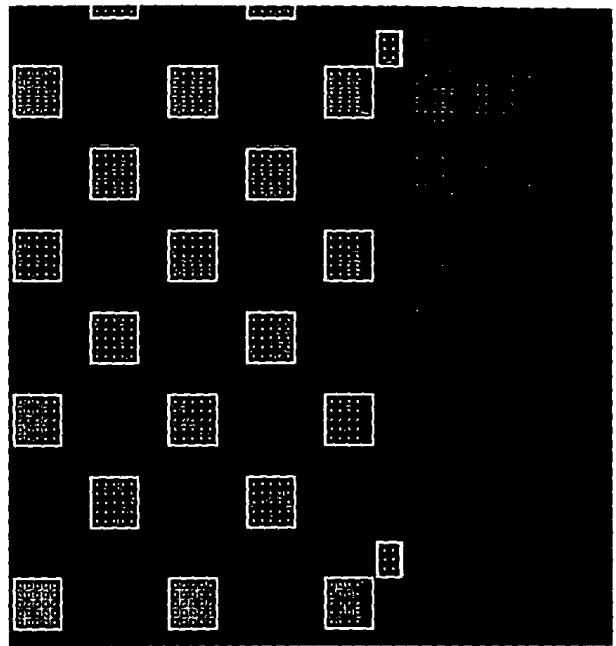


← 10 μm →

Small area of Metal 5 (0.04Ω/Sq) ball contact pad 'checkerboard' to same scale as previous drawings. Red area covering left 22μm of drawing is the right side of a source M5 ball contact pad, while the blue area (right 13μm) is the left side of a drain M5 pad. These M5 ball contact pads are nominally 250μm square using standard flip-chip ball pitches, or 100μm or less using advanced 'SHOCC' ball pitches.

FIG. 5B

Drain Metal 4 Plan (Blue) & (Red) Source M4 Feedthru Patches with Vias to Metal 5 Contacts

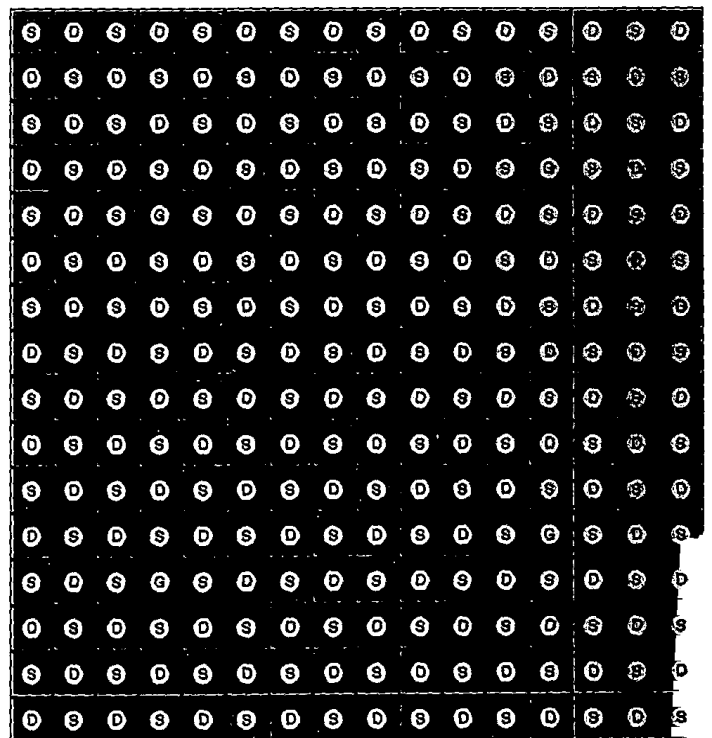


← 10 μm →

Metal 4 (0.08Ω/Sq) drain plane (blue) with isolated M4 source feedthru pads (red) with M4/M5 via patches carrying current from the M3 source plane to M5 source 'checkerboard' pad contact area over left 22μm of area drawn. Since right 13μm of area shown has drain M5, this area is covered with M4/M5 vias connecting M4 drain plane with M5 drain pads.

FIG. 5D

Full Chip View of Solder Balls and 'Checkerboard' Source, Drain & Gate Metal 5 Ball Contact Area



← 1 mm →

Full chip view of 4mm x 4mm die (scale 100x larger than previous drawing showing Metal 5 (0.04Ω/Sq) source (red), drain (blue) and gate (green) 'checkerboard' of ball contact pads with solder balls at their centers. While 250μm flip-chip ball pitch is shown, reducing to ≤100μm would improve metal resistance

FIG. 6A

Richard Egan & Len Schepers 9/5/90

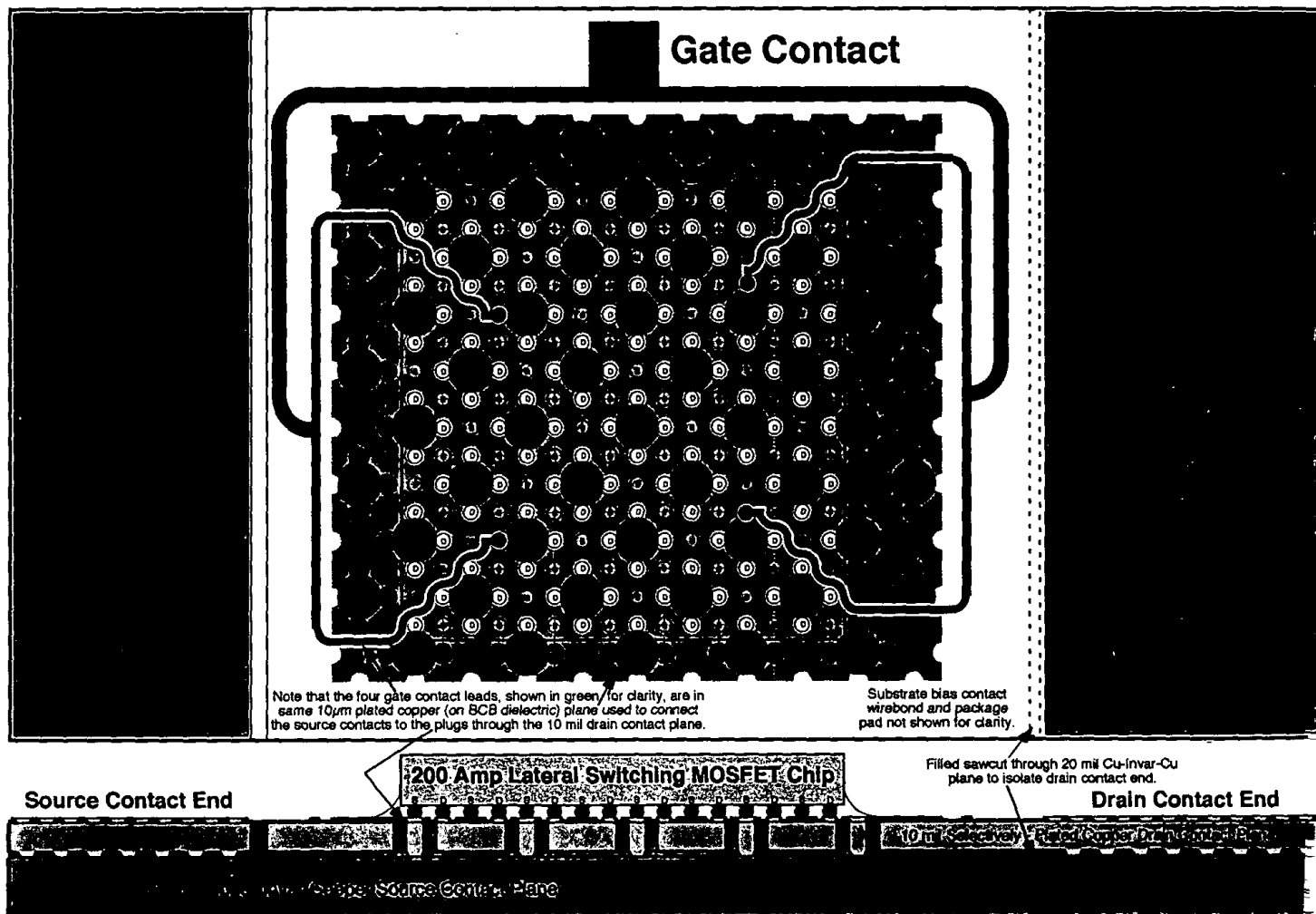
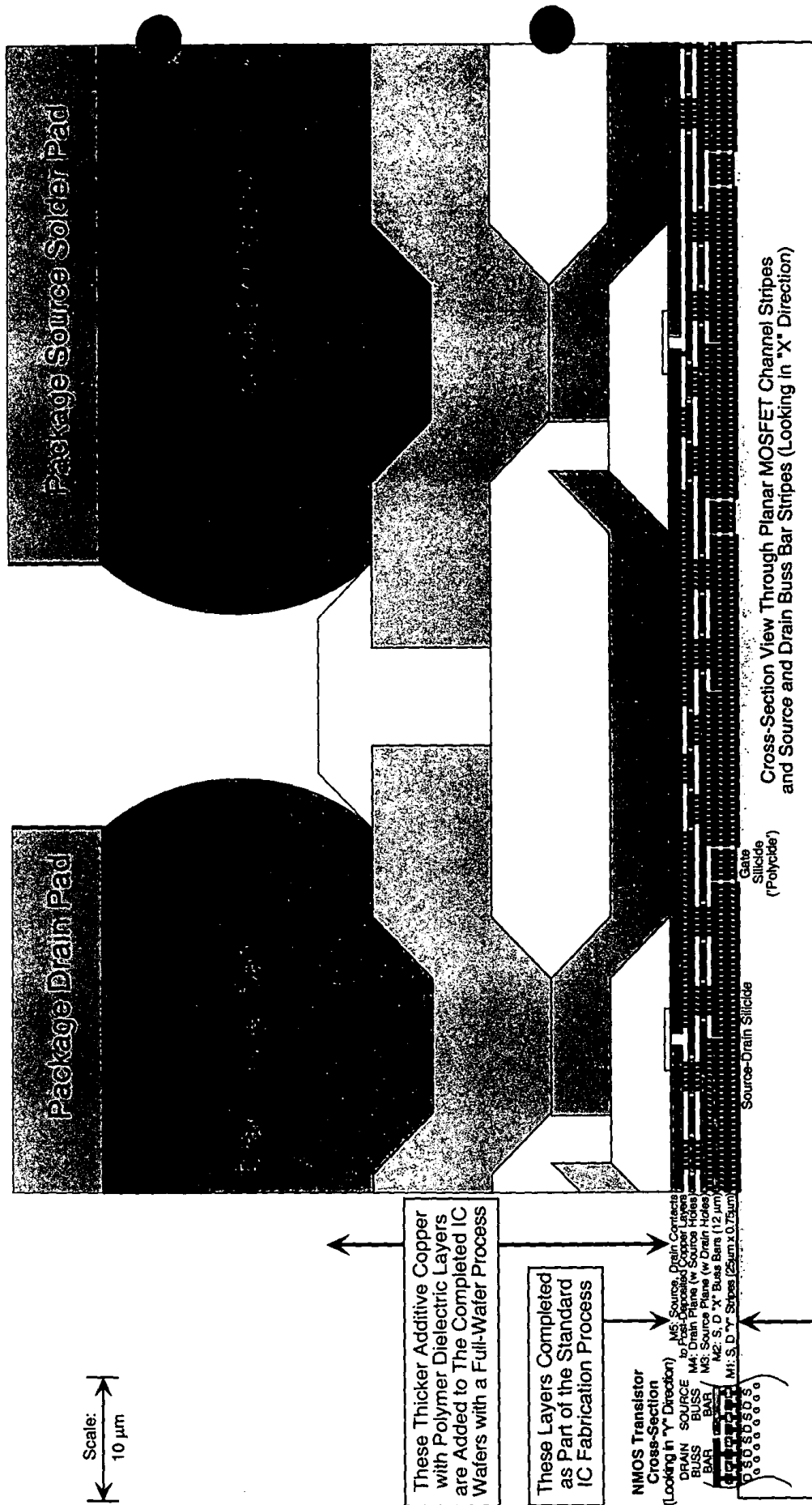


FIG. 6B

Cross-Section of 200 Amp Planar Switching MOSFET Chip After Full-Wafer Deposition of Additive Copper/Polymer Interconnect Layers on Completed IC Wafer



Silicon NMOS FET Substrate
(thickness not drawn to scale)

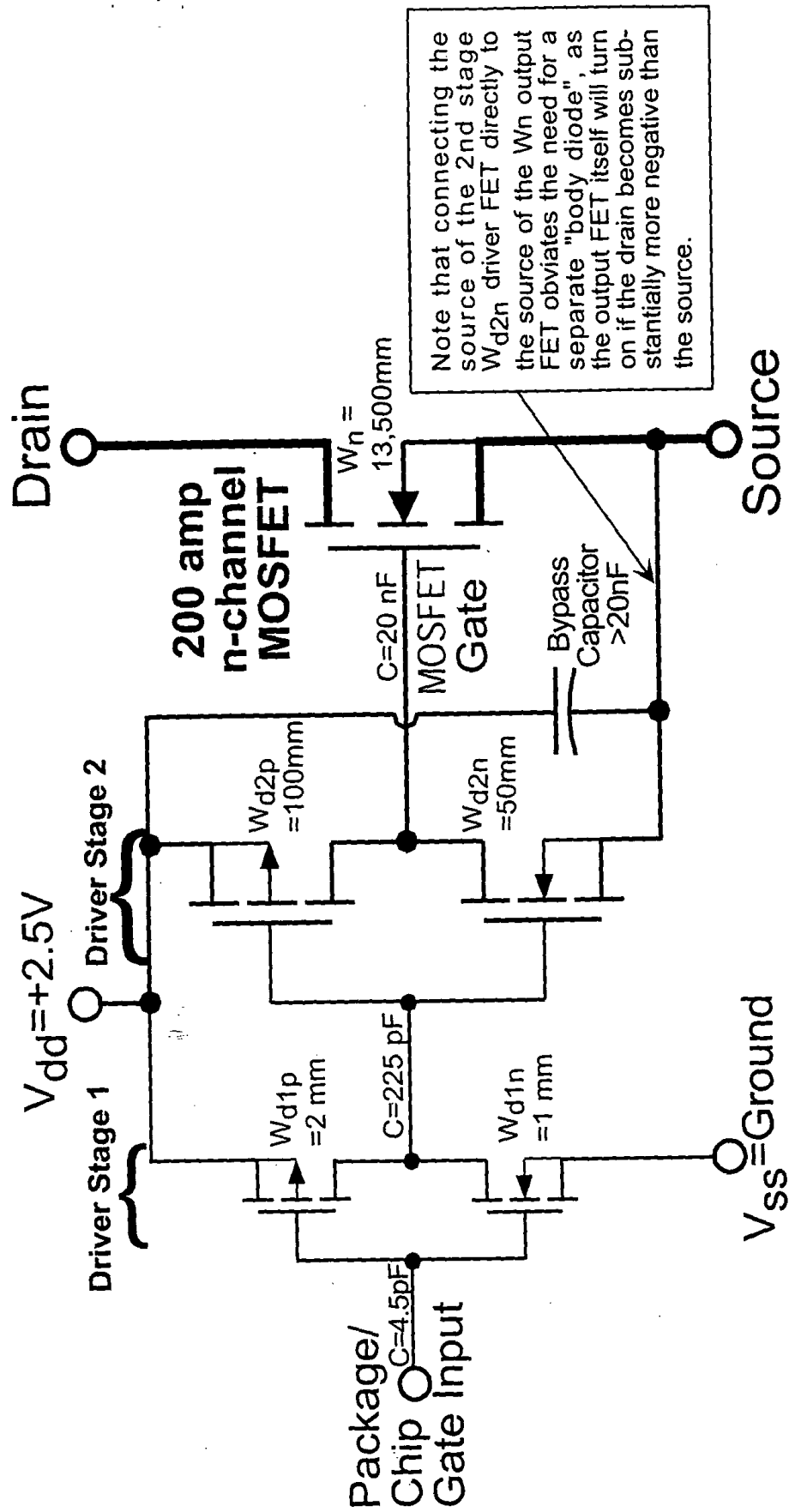


FIG. 8

Alternate "Stripe" Layout of 200 amp NMOS Switching FET Chip with Gate Drive Amplifier for Compatibility with Very Low Resistance Vertically Laminated Package

Full Chip View of Solder Balls and Source, Drain & Gate Metal 5 Ball Contact Areas

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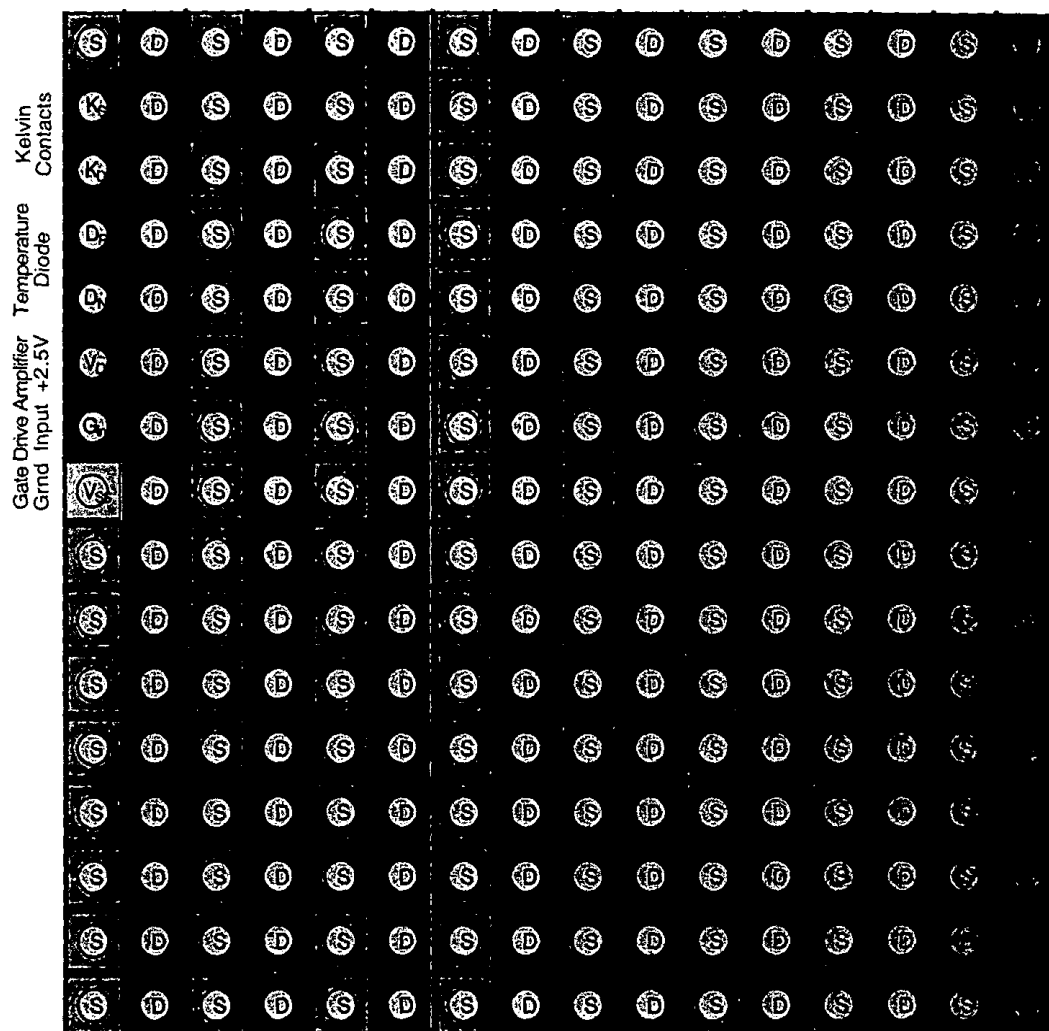
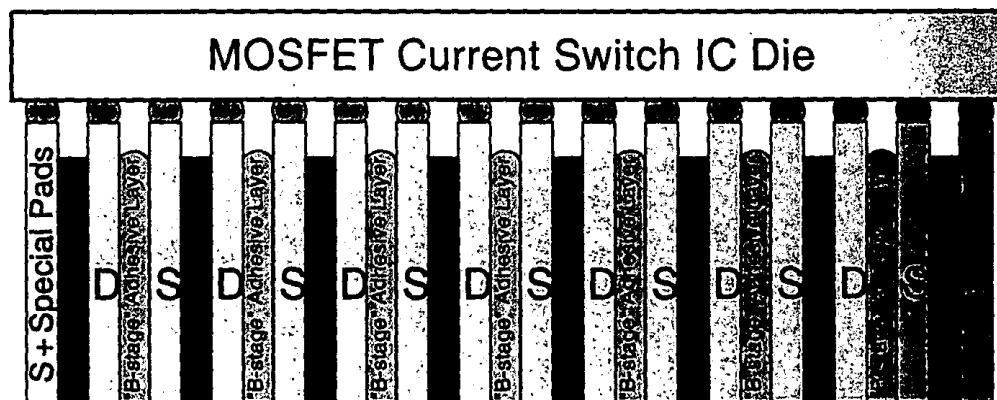


FIG. 9A

Package Height may be Increased Indefinitely for Lower Package Resistance



Side View of Mating Very Low-R Vertical Laminate Package

FIG. 9B

Richard C. Eden
8/14/89
M1: S A D 25um Y Links M2: X Strips S & D=24um each G=2.5um M3: S Plane (w S's) M4: D Plane (w S's) M5: S, D Pad Checkerboard

	μm
Lambda (Lgd2)=	0.125
Source Width=	0.75

	µm	µm	µm
Cave Jumper via	28	38.40	38.40
Vertical Pitch Pys		Silicon/Translator:	
		µm	50.48
			On-Chip Memory Elements
			51.96

Drain Via Patch vs Via Patch Blank Y-axis	2.5 5	µm	700	A min 50% DC Biaser (M/min)	3.008	2.854
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# of Vias per Patch	Via/Patch	0.8 μ m Aluminum	Number of Copper/BCB Layers
25	Q/25q	0.08	1
Sheet R for M1-M4			

Part	Q/Sq	Q/Sq	Thickness=0.3 ball pitch	Total MOSFET Width (meters)=
Solder Ball Sheet A	0.00283	0.00283		12.5

	Number Bats on CNP	Balls/Row	Sales/Ship
Eggs MS B2/A1 ratio	16	254	?

Layer(s)	Material	Thickness (mm)
1	Copper	0.035
2	Dielectric	0.127
3	Copper	0.035
4	Dielectric	0.127
5	Copper	0.035
6	Dielectric	0.127
7	Copper	0.035
8	Dielectric	0.127
9	Copper	0.035
10	Dielectric	0.127
11	Copper	0.035
12	Dielectric	0.127
13	Copper	0.035
14	Dielectric	0.127
15	Copper	0.035
16	Dielectric	0.127
17	Copper	0.035
18	Dielectric	0.127
19	Copper	0.035
20	Dielectric	0.127
21	Copper	0.035
22	Dielectric	0.127
23	Copper	0.035
24	Dielectric	0.127
25	Copper	0.035
26	Dielectric	0.127
27	Copper	0.035
28	Dielectric	0.127
29	Copper	0.035
30	Dielectric	0.127
31	Copper	0.035
32	Dielectric	0.127
33	Copper	0.035
34	Dielectric	0.127
35	Copper	0.035
36	Dielectric	0.127
37	Copper	0.035
38	Dielectric	0.127
39	Copper	0.035
40	Dielectric	0.127
41	Copper	0.035
42	Dielectric	0.127
43	Copper	0.035
44	Dielectric	0.127
45	Copper	0.035
46	Dielectric	0.127
47	Copper	0.035
48	Dielectric	0.127
49	Copper	0.035
50	Dielectric	0.127
51	Copper	0.035
52	Dielectric	0.127
53	Copper	0.035
54	Dielectric	0.127
55	Copper	0.035
56	Dielectric	0.127
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81	Copper	0.035
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83	Copper	0.035
84	Dielectric	0.127
85	Copper	0.035
86	Dielectric	0.127
87	Copper	0.035
88	Dielectric	0.127
89	Copper	0.035
90	Dielectric	0.127
91	Copper	0.035
92	Dielectric	0.127
93	Copper	0.035
94	Dielectric	0.127
95	Copper	0.035
96	Dielectric	0.127
97	Copper	0.035
98	Dielectric	0.127
99	Copper	0.035
100	Dielectric	0.127
101	Copper	0.035
102	Dielectric	0.127
103	Copper	0.035
104	Dielectric	0.127
105	Copper	0.035
106	Dielectric	0.127
107	Copper	0.035
108	Dielectric	0.127
109	Copper	0.035
110	Dielectric	0.127
111	Copper	0.035
112	Dielectric	0.127
113	Copper	0.035
114	Dielectric	0.127
115	Copper	0.035
116	Dielectric	0.127
117	Copper	0.035
118	Dielectric	0.127
119	Copper	0.035
120	Dielectric	0.127
121	Copper	

	cm	mm
Thick Plated Cu Tm	0.0254	10
Thick Plated Cu Sheet F	6.7E-06	0.000261

	mm	inches
Total Package Length	1.28	0.050396
Effective Plane nos	0.6	0.0236
2/3 of chip to far contact pad ± 0.75mm		

	CU	INVS
CU-Invar-Cu Sheet R	0.0006	0.034666
CU-Invar-Cu Sheet R	3.3E-06	0.034666

Component	Parameter	Units
		Ohms

Source, Drain	R_g, R_d	$W-\mu m$	$R_s =$	$R_d =$	$R_s + R_d =$	0.000030
Source, Drain	R_g, R_d	190	$R_s =$	$R_d =$	$R_s + R_d =$	0.000030

	RVD1	W/Cut	Cuts	RVO1s=	RV01d=	RM1s+d=	RM1d=	RM1s+d=
Slice-M1 V ₈		7.5	1250000		0.0000006		0.0000006	0.000000
M1 Strps (S.D)		0.08	250000		2.66687E-08		2.66687E-08	5.33333E

[illegible]

M3-M4 Via (S)	Patches	Patches
M3-M4 Via (S)	RV34g=	RV34g=
M4-M5 Via (S)	RV46g=	RV46g=
M4-M5 Via (S)	RV48g=	RV48g=

Model	RMSE	RMSEd	RMSEe
M3 Spread to MS (3)	0.0071428	0.0070250	0.0070250
M5 Spread to Bail (0)	0.0238294	0.0238294	0.0238294
RM6d	0.0071428	0.0070250	0.0070250
RM6e	0.0238294	0.0238294	0.0238294
RM7d	0.0071428	0.0070250	0.0070250
RM7e	0.0238294	0.0238294	0.0238294
RM8d	0.0071428	0.0070250	0.0070250
RM8e	0.0238294	0.0238294	0.0238294
RM9d	0.0071428	0.0070250	0.0070250
RM9e	0.0238294	0.0238294	0.0238294
RM10d	0.0071428	0.0070250	0.0070250
RM10e	0.0238294	0.0238294	0.0238294
RM11d	0.0071428	0.0070250	0.0070250
RM11e	0.0238294	0.0238294	0.0238294
RM12d	0.0071428	0.0070250	0.0070250
RM12e	0.0238294	0.0238294	0.0238294
RM13d	0.0071428	0.0070250	0.0070250
RM13e	0.0238294	0.0238294	0.0238294
RM14d	0.0071428	0.0070250	0.0070250
RM14e	0.0238294	0.0238294	0.0238294
RM15d	0.0071428	0.0070250	0.0070250
RM15e	0.0238294	0.0238294	0.0238294
RM16d	0.0071428	0.0070250	0.0070250
RM16e	0.0238294	0.0238294	0.0238294
RM17d	0.0071428	0.0070250	0.0070250
RM17e	0.0238294	0.0238294	0.0238294
RM18d	0.0071428	0.0070250	0.0070250
RM18e	0.0238294	0.0238294	0.0238294
RM19d	0.0071428	0.0070250	0.0070250
RM19e	0.0238294	0.0238294	0.0238294
RM20d	0.0071428	0.0070250	0.0070250
RM20e	0.0238294	0.0238294	0.0238294
RM21d	0.0071428	0.0070250	0.0070250
RM21e	0.0238294	0.0238294	0.0238294
RM22d	0.0071428	0.0070250	0.0070250
RM22e	0.0238294	0.0238294	0.0238294
RM23d	0.0071428	0.0070250	0.0070250
RM23e	0.0238294	0.0238294	0.0238294
RM24d	0.0071428	0.0070250	0.0070250
RM24e	0.0238294	0.0238294	0.0238294
RM25d	0.0071428	0.0070250	0.0070250
RM25e	0.0238294	0.0238294	0.0238294
RM26d	0.0071428	0.0070250	0.0070250
RM26e	0.0238294	0.0238294	0.0238294
RM27d	0.0071428	0.0070250	0.0070250
RM27e	0.0238294	0.0238294	0.0238294
RM28d	0.0071428	0.0070250	0.0070250
RM28e	0.0238294	0.0238294	0.0238294
RM29d	0.0071428	0.0070250	0.0070250
RM29e	0.0238294	0.0238294	0.0238294
RM30d	0.0071428	0.0070250	0.0070250
RM30e	0.0238294	0.0238294	0.0238294
RM31d	0.0071428	0.0070250	0.0070250
RM31e	0.0238294	0.0238294	0.0238294
RM32d	0.0071428	0.0070250	0.0070250
RM32e	0.0238294	0.0238294	0.0238294
RM33d	0.0071428	0.0070250	0.0070250
RM33e	0.0238294	0.0238294	0.0238294
RM34d	0.0071428	0.0070250	0.0070250
RM34e	0.0238294	0.0238294	0.0238294
RM35d	0.0071428	0.0070250	0.0070250
RM35e	0.0238294	0.0238294	0.0238294
RM36d	0.0071428	0.0070250	0.0070250
RM36e	0.0238294	0.0238294	0.0238294
RM37d	0.0071428	0.0070250	0.0070250
RM37e			

	Belle	RSB=	RSRd=	RSRPd=	RSPS+d=	2.1008E
Solder Ball Resistance	RSB	0.0013446	(Y)Ball	126	0	
Cable Rod Resistance	RCRD	0	(Y)Rod	126	0	

Model	RS/PMC	1/Pad	50%	4
Mild Source Pad R	0.0046274	1/Pad	50%	4
Stud Source Pad R	0	1/Pad	26%	1

	RTCuD	RTCuA	RTCuB	RTCuC	RTCuE	RTCuF	RTCuG	RTCuH	RTCuI	RTCuJ	RTCuK	RTCuL	RTCuM	RTCuN	RTCuO	RTCuP	RTCuQ	RTCuR	RTCuS	RTCuT	RTCuU	RTCuV	RTCuW	RTCuX	RTCuY	RTCuZ	RTCuAA	RTCuAB	RTCuAC	RTCuAD	RTCuAE	RTCuAF	RTCuAG	RTCuAH	RTCuAI	RTCuAJ	RTCuAK	RTCuAL	RTCuAM	RTCuAN	RTCuAO	RTCuAP	RTCuAQ	RTCuAR	RTCuAS	RTCuAT	RTCuAU	RTCuAV	RTCuAW	RTCuAX	RTCuAY	RTCuAZ	RTCuBA	RTCuBB	RTCuBC	RTCuBD	RTCuBE	RTCuBF	RTCuBG	RTCuBH	RTCuBI	RTCuBJ	RTCuBK	RTCuBL	RTCuBM	RTCuBN	RTCuBO	RTCuBP	RTCuBQ	RTCuBR	RTCuBS	RTCuBT	RTCuBU	RTCuBV	RTCuBW	RTCuBX	RTCuBY	RTCuBZ	RTCuCA	RTCuCB	RTCuCC	RTCuCD	RTCuCE	RTCuCF	RTCuCG	RTCuCH	RTCuCI	RTCuCJ	RTCuCK	RTCuCL	RTCuCM	RTCuCN	RTCuCO	RTCuCP	RTCuCQ	RTCuCR	RTCuCS	RTCuCT	RTCuCU	RTCuCV	RTCuCW	RTCuCX	RTCuCY	RTCuCZ	RTCuDA	RTCuDB	RTCuDC	RTCuDD	RTCuDE	RTCuDF	RTCuDG	RTCuDH	RTCuDI	RTCuDJ	RTCuDK	RTCuDL	RTCuDM	RTCuDN	RTCuDO	RTCuDP	RTCuDQ	RTCuDR	RTCuDS	RTCuDT	RTCuDU	RTCuDV	RTCuDW	RTCuDX	RTCuDY	RTCuDZ	RTCuEA	RTCuEB	RTCuEC	RTCuED	RTCuEE	RTCuEF	RTCuEG	RTCuEH	RTCuEI	RTCuEJ	RTCuEK	RTCuEL	RTCuEM	RTCuEN	RTCuEO	RTCuEP	RTCuEQ	RTCuER	RTCuES	RTCuET	RTCuEU	RTCuEV	RTCuEW	RTCuEX	RTCuEY	RTCuEZ	RTCuFA	RTCuFB	RTCuFC	RTCuFD	RTCuFE	RTCuFF	RTCuFG	RTCuFH	RTCuFI	RTCuFJ	RTCuFK	RTCuFL	RTCuFM	RTCuFN	RTCuFO	RTCuFP	RTCuFQ	RTCuFR	RTCuFS	RTCuFT	RTCuFU	RTCuFV	RTCuFW	RTCuFX	RTCuFY	RTCuFZ	RTCuGA	RTCuGB	RTCuGC	RTCuGD	RTCuGE	RTCuGF	RTCuGG	RTCuGH	RTCuGI	RTCuGJ	RTCuGK	RTCuGL	RTCuGM	RTCuGN	RTCuGO	RTCuGP	RTCuGQ	RTCuGR	RTCuGS	RTCuGT	RTCuGU	RTCuGV	RTCuGW	RTCuGX	RTCuGY	RTCuGZ	RTCuHA	RTCuHB	RTCuHC	RTCuHD	RTCuHE	RTCuHF	RTCuHG	RTCuHH	RTCuHI	RTCuHJ	RTCuHK	RTCuHL	RTCuHM	RTCuHN	RTCuHO	RTCuHP	RTCuHQ	RTCuHR	RTCuHS	RTCuHT	RTCuHU	RTCuHV	RTCuHW	RTCuHX	RTCuHY	RTCuHZ	RTCuIA	RTCuIB	RTCuIC	RTCuID	RTCuIE	RTCuIF	RTCuIG	RTCuIH	RTCuII	RTCuIJ	RTCuIK	RTCuIL	RTCuIM	RTCuIN	RTCuIO	RTCuIP	RTCuIQ	RTCuIR	RTCuIS	RTCuIT	RTCuIU	RTCuIV	RTCuIW	RTCuIX	RTCuIY	RTCuIZ	RTCuJA	RTCuJB	RTCuJC	RTCuJD	RTCuJE	RTCuJF	RTCuJG	RTCuJH	RTCuJI	RTCuJJ	RTCuJK	RTCuJL	RTCuJM	RTCuJN	RTCuJO	RTCuJP	RTCuJQ	RTCuJR	RTCuJS	RTCuJT	RTCuJU	RTCuJV	RTCuJW	RTCuJX	RTCuJY	RTCuJZ	RTCuKA	RTCuKB	RTCuKC	RTCuKD	RTCuKE	RTCuKF	RTCuKG	RTCuKH	RTCuKI	RTCuKJ	RTCuKK	RTCuKL	RTCuKM	RTCuKN	RTCuKO	RTCuKP	RTCuKQ	RTCuKR	RTCuKS	RTCuKT	RTCuKU	RTCuKV	RTCuKW	RTCuKX	RTCuKY	RTCuKZ	RTCuLA	RTCuLB	RTCuLC	RTCuLD	RTCuLE	RTCuLF	RTCuLG	RTCuLH	RTCuLI	RTCuLJ	RTCuLK	RTCuLL	RTCuLM	RTCuLN	RTCuLO	RTCuLP	RTCuLQ	RTCuLR	RTCuLS	RTCuLT	RTCuLU	RTCuLV	RTCuLW	RTCuLX	RTCuLY	RTCuLZ	RTCuMA	RTCuMB	RTCuMC	RTCuMD	RTCuME	RTCuMF	RTCuMG	RTCuMH	RTCuMI	RTCuMJ	RTCuMK	RTCuML	RTCuMM	RTCuMN	RTCuMO	RTCuMP	RTCuMQ	RTCuMR	RTCuMS	RTCuMT	RTCuMU	RTCuMV	RTCuMW	RTCuMX	RTCuMY	RTCuMZ	RTCuNA	RTCuNB	RTCuNC	RTCuND	RTCuNE	RTCuNF	RTCuNG	RTCuNH	RTCuNI	RTCuNJ	RTCuNK	RTCuNL	RTCuNM	RTCuNN	RTCuNO	RTCuNP	RTCuNQ	RTCuNR	RTCuNS	RTCuNT	RTCuNU	RTCuNV	RTCuNW	RTCuNX	RTCuNY	RTCuNZ	RTCuOA	RTCuOB	RTCuOC	RTCuOD	RTCuOE	RTCuOF	RTCuOG	RTCuOH	RTCuOI	RTCuOJ	RTCuOK	RTCuOL	RTCuOM	RTCuON	RTCuOO	RTCuOP	RTCuOQ	RTCuOR	RTCuOS	RTCuOT	RTCuOU	RTCuOV	RTCuOW	RTCuOX	RTCuOY	RTCuOZ	RTCuPA	RTCuPB	RTCuPC	RTCuPD	RTCuPE	RTCuPF	RTCuPG	RTCuPH	RTCuPI	RTCuPJ	RTCuPK	RTCuPL	RTCuPM	RTCuPN	RTCuPO	RTCuPP	RTCuPQ	RTCuPR	RTCuPS	RTCuPT	RTCuPU	RTCuPV	RTCuPW	RTCuPX	RTCuPY	RTCuPZ	RTCuQA	RTCuQB	RTCuQC	RTCuQD	RTCuQE	RTCuQF	RTCuQG	RTCuQH	RTCuQI	RTCuQJ	RTCuQK	RTCuQL	RTCuQM	RTCuQN	RTCuQO	RTCuQP	RTCuQQ	RTCuQR	RTCuQS	RTCuQT	RTCuQU	RTCuQV	RTCuQW	RTCuQX	RTCuQY	RTCuQZ	RTCuRA	RTCuRB	RTCuRC	RTCuRD	RTCuRE	RTCuRF	RTCuRG	RTCuRH	RTCuRI	RTCuRJ	RTCuRK	RTCuRL	RTCuRM	RTCuRN	RTCuRO	RTCuRP	RTCuRQ	RTCuRR	RTCuRS	RTCuRT	RTCuRU	RTCuRV	RTCuRW	RTCuRX	RTCuRY	RTCuRZ	RTCuSA	RTCuSB	RTCuSC	RTCuSD	RTCuSE	RTCuSF	RTCuSG	RTCuSH	RTCuSI</
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